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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/622,150	07/16/2003	Matthew Louis Courcy	NSC-P05579	1923
75	90 02/14/2006		EXAM	INER
WAGNER, MURABITO & HAO LLP			WILLIAMS, HOWARD L	
Third Floor Two North Mar	kat Straat		ART UNIT	PAPER NUMBER
San Jose, CA 95113			2819	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/622,150	COURCY, MATTHEW LOUIS				
Office Action Summary	Examiner	Art Unit				
	Howard L. Williams	2819				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
 1) Responsive to communication(s) filed on <u>03 January 2006</u>. 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i>, 1935 C.D. 11, 453 O.G. 213. 						
Disposition of Claims						
4) Claim(s) 1-3,5-9,11-15,17-21 and 23 is/are penda) Of the above claim(s) is/are withdraw 5) Claim(s) is/are allowed. 6) Claim(s) 1-3,5-9,11-15,17-21 and 23 is/are rejet 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or Application Papers	vn from consideration.					
9) The specification is objected to by the Examiner.						
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:					

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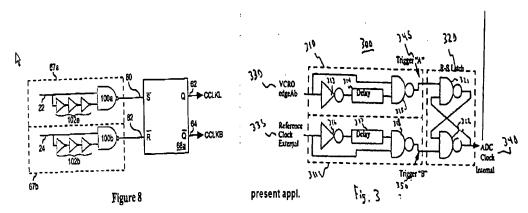
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, and 5 are rejected under 35 U.S.C. 102(b) as anticipated by U.S. P.A.P. 20020017936 A1 to Stark et al or Eitrheim et al. (EP 570158 A2).

Stark in figure 8 discloses: edge detectors (67a & 67b) and latch/S-R flip flop (66a).



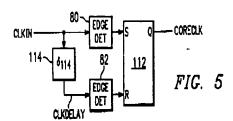
Stark's figure 8 (on the left above) has the same configuration as figure 3 of the present application since the inverters 102a and 102b provide delay circuits. The inputs (22, 24) to the Stark edge detectors are complementary clock signals and 180 degrees out of phase. In the terms of signal period and duty cycle would be one-half clock period delayed phase. Stark's circuit also inherently provides an output clock that is independent of the duty cycle of the input given the similar construction of the circuit to that of Eitrheim et al. (see below)

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Eitrheim et al. in figure 5 discloses a clock generation circuit that includes an

EP 0 570 158 A2



edge detector 80, conditioning circuit 114 and an R-S latch. Eitrheim also discloses that the clock output ("CORECLK" in the figure) is independent of the duty cycle of the input clock (abstract and col. 11, line 31).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-9, 11, 12 are rejected under 35 U.S.C. 103(a) as unpatentable over U.S. P.A.P. 20020017936 A1 to Stark et al. in view of Huynh (US 20030107432 A1) or Eitrheim et al. (EP 570158 A2) in view of Huynh (US 20030107432 A1).

Stark et al. does not mention ADC systems in particular but discloses two edge detectors side by side to the S input and R input, respectively, of an S-R flip-flop or latch, similar to applicants' embodiment. The clock duty cycle regulator of Stark et al. would have been an obvious choice to provide a 50% duty cycle clock signal because use of the a cleanly squared clock signal would provide a suitable clock to enable Huynh to achieve the desired well-timed output once each cycle thus increasing the circuit through-put and improving the applications such as data recovery.

Eitrheim et al. does not mention ADC systems in particular but discloses two edge detectors side by side to the S input and R input, respectively, of an S-R flip-flop

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or latch, similar to applicants' embodiment. The clock duty cycle regulator of Eitrheim et al. would have been an obvious choice to provide a 50% duty cycle clock signal because use of the a cleanly squared clock signal would provide a suitable clock to enable Huynh to achieve the desired well-timed output once each cycle thus increasing the circuit through-put and improving the applications such as data recovery.

Claims 13-15,17,18-21, and 23 are rejected under 35 U.S.C. 103(a) as unpatentable over U.S. P.A.P. 20020017936 A1 to Stark et al. in view of Huynh (US 20030107432 A1) and Davis (US 5394114 A) or Eitrheim et al. (EP 570158 A2) in view of Huynh (US 20030107432 A1) and Davis (US 5394114 A).

Stark discloses a clock generation circuit, duty cycle converter/corrector including two edge detectors supplying an S-R Flip-Flop serving as the claimed time generator or latch. Huynh supplies (from above) reasonable suggestion of well-timed clocks for an ADC. Stark does not elaborate on the clock generation circuit so does not disclose the claimed VCRO. Voltage controlled ring oscillators though are widely used to generate multiple-phased clock signals from which an appropriately phased clock signal is selected. Davis discloses a voltage controlled ring oscillator to generate out of phase clock signals.

Eitrheim et al. receives the clock signal and feeds it to a programmable delay to produce a signal with a desired phase delay from the external clock. While not the claimed VCRO it is noted that the description specifies that numerous elements would interchangeably serve to provide the delayed/inverted clock (pg. 9 of specification). As such it would have been obvious to employ a VCO to generate the delayed clock because VCOs are well known and widely used to generate multiple phased clock signals from which an appropriately phased clock signal may be selected.

The remarks filed 03 January 2006 have been fully considered but are not found persuasive. The remarks urge that Stark in discussing the cross point duty cycle being equal (remarks page 12) to the edge duty cycle of a pair of input signals is teaching away from the claimed invention is not persuasive. The circuit of Stark receives a clock

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and inverted clock similar to the circuit of this application. Stark applies both the clock and the conditioned signal (inverted or complemented clock) to respective edge detectors, which in turn are connected to an S-R latch that generates the output clock signal. Accordingly, Stark would also provide the output clock with independence from the duty cycle of the input clock. The remaining remarks seem only to reiterate this point saying that the secondary references to cure the asserted deficiency of Stark.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Howard L. Williams at telephone number 571.272.1815. The Patent and Trademark Office has a new central facsimile number for application specific correspondence intended for entry, it is 703-872-9306.

2/7/06 Voice 571.272.1815 Howard L. Williams Primary Examiner Art Unit 2819